IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant(s): | Om P. Agrawal; Bai Nguyen; Kuang Chi; Brad Sharpe-Geisler; Giap Tran | | |
| Assignee: | Lattice Semiconductor Corporation | | |
| Title: | Scalable Serializer-Deserializer Architecture And Programmable Interface | | |
| Serial No.: | 10/619,645 | Filing Date: | 07/14/2003 |
| Examiner: | Jason Crawford | Group Art Unit: | 2819 |
| Docket No.: | M-15135 US | Confirmation No.: | 9559 |

Irvine, California
March 20, 2006

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**37 C.F.R. 1.131 DECLARATION**

Dear Sir:

We, Om P. Agrawal, Bai Nguyen, Kuang Chi, Brad Sharpe-Geisler, and Giap Tran, declare as follows:

1. We were or are currently employed at Lattice Semiconductor Corporation and are the inventors for the above-referenced patent application entitled "Scalable Serializer-Deserializer Architecture and Programmable Interface" (hereinafter referred to as "the Patent Application").

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

2. Within the United States, we conceived and reduced to practice the invention disclosed in the Patent Application prior to April 28, 2003, the effective date of U.S. Patent No. 6,894,530.

3. The reduction to practice (referred to in paragraph 2) resulted from the implementation of the invention (e.g., the invention as disclosed in the Patent Application and recited in Claims 1-20 of the Patent Application) within an ispXPGA product offered by Lattice Semiconductor Corporation.

4. The ispXPGA product was first publicly announced by Lattice Semiconductor Corporation in a press release on July 15, 2002, a copy of which is attached as Exhibit A.

5. Samples of the ispXPGA product were first released to customers in March 2003 and details of the released product were disclosed in a published Preliminary Data Sheet entitled "ispXPGA Family" dated March 2003 by Lattice Semiconductor Corporation (referred to in the Patent Application on page 15, lines 15-20 and herein referred to as "the Preliminary Data Sheet," a copy of which is attached as Exhibit B).

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CHEN & HEID LLP

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6. The Preliminary Data Sheet shows a successful exemplary implementation of the invention in the ispXPGA product prior to April 28, 2003.

7. Alternatively to paragraphs 2 through 6, a patent application draft (hereinafter referred to as "the Patent Application Draft") corresponding to the Patent Application was completed prior to April 28, 2003 (a copy of the letter dated April 7, 2003 enclosing the Patent Application Draft to one of the inventors is attached as Exhibit C).

8. The Patent Application Draft was reviewed by the inventors and approved for filing by Lattice Semiconductor Corporation, with due diligence during the time from the completion of the Patent Application Draft prior to April 28, 2003 to the filing of the Patent Application on July 14, 2003.

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations,

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FAX (949) 752-7049

or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

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|---|---|---|---|
| Full name of first joint inventor: | Om P. Agrawal | | |
| Inventor's Signature: | | Date: | |

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| Full name of second joint inventor: | Bai Nguyen | | |
| Inventor's Signature: | | Date: | 3/16/06 |

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| Full name of third joint inventor: | Kuang Chi | | |
| Inventor's Signature: | Kuang-Kai Chi | Date: | 3/16/06 |

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| Full name of fourth joint inventor: | Brad Sharpe-Geisler | | |
| Inventor's Signature: | | Date: | 3/16/06 |

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|---|---|---|---|
| Full name of fourth joint inventor: | Giap Tran | | |
| Inventor's Signature: | | Date: | 3/16/06 |

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2403 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

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|---|---|---|---|
| Full name of 1 joint inventor: | Om P. Agrawal | | |
| Inventor's Signature: | | Date: | 3/20/06 |

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|---|---|---|---|
| Full name of second joint inventor: | Bai Nguyen | | |
| Inventor's Signature: | | Date: | |

| | | | |
|---|---|---|---|
| Full name of third joint inventor: | Kuang Chi | | |
| Inventor's Signature: | | Date: | |

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|---|---|---|---|
| Full name of fourth joint inventor: | Brad Sharpe-Geisler | | |
| Inventor's Signature: | | Date: | |

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|---|---|---|---|
| Full name of fourth joint inventor: | Giap Tran | | |
| Inventor's Signature: | | Date: | |